WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a heat sink comprising a bottom surface exposed to the outside and an upper surface opposed to said bottom surface;

an insulating substrate jointed to said upper surface of said heat sink;

a conductive plate jointed to an upper surface of said insulating substrate;

a first semiconductor chip comprising a first main electrode electrically connected through a first conductive layer to an upper surface of said conductive plate, and a second main electrode opposed to and having a smaller area than said first main electrode;

a second semiconductor chip comprising a first main electrode electrically connected through a second conductive layer to and having a smaller area than said second main electrode of said first semiconductor chip, and a second main electrode opposed to said first main electrode; and

a container enclosing said heat sink except an exposed portion of said bottom surface, said insulating substrate, said conductive plate, said first semiconductor chip and said second semiconductor chip in its interior space,

wherein a portion above said second main electrode of said second semiconductor chip is said interior space of said container, and

wherein a base material of said second semiconductor chip is a wide gap semiconductor having a greater interband energy gap than silicon.

2. The semiconductor device according to claim 1, wherein

a base material of said first semiconductor chip is also said wide gap semiconductor.

3. The semiconductor device according to claim 1, wherein

said first semiconductor chip is located on a first region of said upper surface of said conductive plate with said first conductive layer sandwiched in between,

said semiconductor device further comprising:

another first semiconductor chip comprising a first main electrode electrically connected through another first conductive layer to a second region of said upper surface of said conductive plate, and a second main electrode opposed to and having a smaller area than said first main electrode; and

another second semiconductor chip comprising a first main electrode electrically connected through another second conductive layer to and having a smaller area than said second main electrode of said another first semiconductor chip, and a second main electrode opposed to said first main electrode,

wherein said container also encloses said another first semiconductor chip and said another second semiconductor chip in said interior space, and

wherein a base material of said another second semiconductor chip is said wide gap semiconductor.

4. A semiconductor device comprising:

a heat sink comprising a bottom surface exposed to the outside and an upper surface opposed to said bottom surface;

an insulating substrate jointed to said upper surface of said heat sink;

a conductive plate jointed to an upper surface of said insulating substrate;

a first semiconductor chip comprising a first main electrode electrically connected through a first conductive layer to a first surface portion of an upper surface of

said conductive plate, and a second main electrode opposed to said first main electrode with respect to a first direction which is equivalent to a direction of a normal to said upper surface of said conductive plate;

a metal base having a first portion and a second portion,

said first portion having a first end which is electrically connected through a second conductive layer to a second surface portion of said upper surface of said conductive plate adjacent to said first surface portion, and extending from said first end to a second end in said first direction,

said second portion being coupled to said second end of said first portion and extending in a second direction orthogonal to said first direction so as to form an L-shape with said first portion;

a second semiconductor chip comprising a first main electrode electrically connected through a third conductive layer to an upper surface of said second portion of said metal base, and a second main electrode opposed to said first main electrode with respect to said first direction; and

a container enclosing said heat sink except an exposed portion of said bottom surface, said insulating substrate, said conductive plate, said first semiconductor chip, said metal base and said second semiconductor chip in its interior space,

wherein a lower surface of said second portion of said metal base is above the level of an upper surface of said second main electrode of said first semiconductor chip, and

wherein a base material of said second semiconductor chip is a wide gap semiconductor having a greater interband energy gap than silicon.

5. The semiconductor device according to claim 4, wherein

a base material of said first semiconductor chip is also said wide gap semiconductor.

6. The semiconductor device according to claim 4, further comprising:

another first semiconductor chip comprising a first main electrode electrically connected through another first conductive layer to a third surface portion of said upper surface of said conductive plate, and a second main electrode opposed to said first main electrode with respect to said first direction;

another metal base having a first portion and a second portion,

said first portion of said another metal base having a first end which is electrically connected through another second conductive layer to a fourth surface portion of said upper surface of said conductive plate adjacent to said third surface portion, and extending from said first end to a second end in said first direction,

said second portion of said another metal base being coupled to said second end of said first portion of said another metal base and extending in said second direction to form an L-shape with said first portion; and

another second semiconductor chip comprising a first main electrode electrically connected through another third conductive layer to an upper surface of said second portion of said another metal base, and a second main electrode opposed to said first main electrode with respect to said first direction,

wherein said container also encloses said another first semiconductor chip, said another base metal and said another second semiconductor chip in said interior space,

wherein a lower surface of said second portion of said another metal base is above the level of an upper surface of said second main electrode of said another first semiconductor chip, and

wherein a base material of said another second semiconductor chip is said wide gap semiconductor.

7. A semiconductor device comprising:

a first conductive base comprising a bottom surface exposed to the outside and an upper surface opposed to said bottom surface;

a first metal base comprising a lower surface on said upper surface of said first conductive base and an upper surface opposed to said lower surface;

a first semiconductor chip comprising a first main electrode located on said upper surface of said first metal base and a second main electrode opposed to said first main electrode;

a second metal base comprising a lower surface on said second main electrode of said first semiconductor chip and an upper surface opposed to said lower surface;

a second semiconductor chip comprising a first main electrode located on said upper surface of said second metal base and a second main electrode opposed to said first main electrode;

a third metal base comprising a lower surface on said second main electrode of said second semiconductor chip and an upper surface opposed to said lower surface;

an insulating substrate comprising a lower surface on said upper surface of said third metal base and an upper surface opposed to said lower surface;

a second conductive base comprising a lower surface on said upper surface of said insulating substrate and an upper surface opposed to said lower surface and exposed to the outside;

a first interconnection electrically connecting said first metal base and said third metal base;

a second interconnection electrically connecting said second metal base and said second conductive base; and

a container enclosing said first conductive base except an exposed portion of said bottom surface, said first metal base, said first semiconductor chip, said second metal base, said second semiconductor chip, said third metal base, said insulating substrate, said second conductive base except an exposed portion of said upper surface, said first interconnection and said second interconnection in its interior space,

wherein said bottom and upper surfaces of said first conductive base have larger areas than said first and second main electrodes of said first semiconductor chip,

wherein said lower and upper surfaces of said second conductive base have larger areas than said first and second main electrodes of said second semiconductor chip, and

wherein a base material of at least one of said first and second semiconductor chips is a wide gap semiconductor having a greater interband energy gap than silicon.

8. The semiconductor device according to claim 7, further comprising:

a bonding layer mechanically joining said upper surface of said first conductive base and said lower surface of said first metal base to each other;

a first conductive layer providing electrical continuity between said upper surface of said first metal base and said first main electrode of said first semiconductor chip;

a second conductive layer providing electrical continuity between said second main electrode of said first semiconductor chip and said lower surface of said second metal base;

a third conductive layer providing electrical continuity between said upper

surface of said second metal base and said first main electrode of said second semiconductor chip;

a fourth conductive layer providing electrical continuity between said second main electrode of said second semiconductor chip and said lower surface of said third metal base;

a first adhesive bonding said upper surface of said third metal base and said lower surface of said insulating substrate; and

a second adhesive bonding said upper surface of said insulating substrate and said lower surface of said second conductive base.

9. The semiconductor device according to claim 7, wherein

a base material of the other of said first and second semiconductor chips is also said wide gap semiconductor.

10. The semiconductor device according to claim 7, wherein

a plurality of semiconductor chip groups, each including one set of said first metal base, said first semiconductor chip, said second metal base, said second semiconductor chip, said third metal base and said insulating substrate, are arranged in parallel between said first conductive base and said second conductive base.